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(54) Process for forming a buried cavity in a semiconductor material wafer

(57) The process comprises the steps of forming, on top of a semiconductor material wafer (10), a holed mask (16) having a lattice structure and comprising a plurality of openings (18) each having a substantially square shape and a side with an inclination of 45° with respect to the flat (110) of the wafer; carrying out an anisotropic etch in TMAH of the wafer (10), using said holed mask (16), thus forming a cavity (20), the cross section of which has the shape of an upside-down isosceles trapezium; and carrying out a chemical vapour deposition (CVD) using TEOS, thus forming a TEOS layer (24) which completely closes the openings of the holed mask (16) and defines a diaphragm (26) overlying the cavity (20) and on which a suspended integrated structure can subsequently be manufactured.

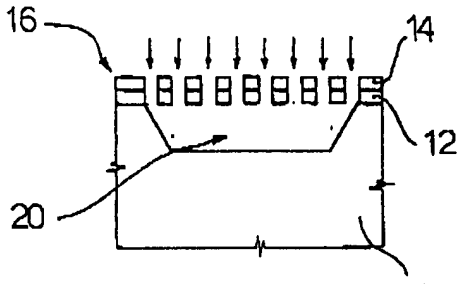

Fig.4c

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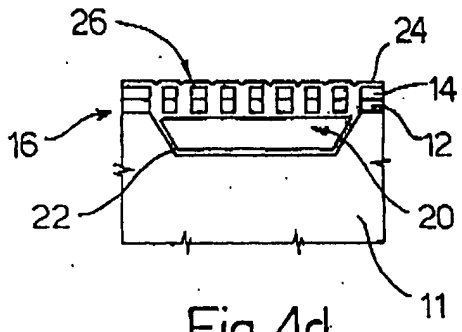

Fig.4d

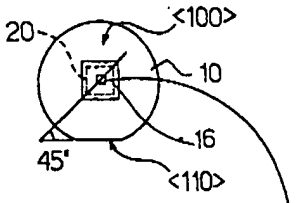

Fig.3

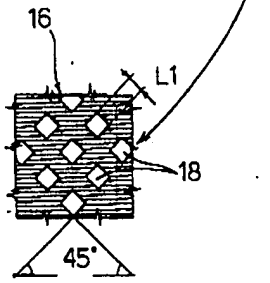

Fig.5

Description

[0001] The present invention regards a process for forming a buried cavity in a semiconductor material wafer.

[0002] As is known, the possibility of manufacturing RF integrated circuits in CMOS or BiCMOS technology would make it possible to obtain lower consumption and lower costs as compared to normal circuits made using gallium arsenide (GaAs).

[0003] At present, however, this possibility is limited by the poor efficiency of the passive elements, and in particular by the inductors, on account of the high parasitic capacitances of the substrate which give rise to low resonance frequencies and preclude the use of high-frequency inductors, and on account of the high conductivity of the substrate, which markedly limits the quality factor Q of the inductor.

[0004] Typical values of the quality factor Q for integrated inductors made on GaAs are of the order of 20 for frequencies of 2 GHz, whereas values of the quality factor Q smaller than 5 are obtained for inductors integrated on high-conductivity silicon substrates (CMOS processes).

[0005] To increase the quality factor Q of integrated inductors in the entire range of interest it is important to reduce both the losses due to the metallizations that make up the coil and losses due to the substrate.

[0006] The losses due to metallizations can be reduced by using aluminium or copper thick layers having relatively high electrical conductivity. However, the skin effect, which, for example, for copper is of the order of 1.5 μm at a frequency of 1 GHz, limits the thickness of the metallization layer in which the current effectively flows. It follows therefore that there is 'no point in using metallization regions having a thickness of over 2 μm to seek to increase the inductor quality factor Q.

[0007] The losses due to the substrate can be reduced by using high-resistivity substrates. However, this solution is not compatible with CMOS technology, which enables only low-resistivity substrates to be obtained.

[0008] One of the techniques used to reduce the losses due to the substrate envisages the formation of a thick oxide layer, namely of over 60 μm, underneath the inductor, which limits the currents inductively generated in the substrate, thus improving the inductor quality factor Q and at the same time enabling higher resonance frequencies to be obtained and wider metallization strips to be used, in this way also reducing ohmic dissipation.

[0009] This technique is schematically illustrated in Figures 1a-1c and envisages the formation, in a wafer 1 of monocrystalline silicon, of deep trenches 2 (Fig. 1a), complete thermal oxidation of the columns 3 of silicon comprised between each pair of contiguous trenches 2 (Fig. 1b), and then chemical vapour deposition (CVD) of a layer of TEOS 4 (tetraethyl orthosilicate), the purpose of which is to complete filling of the trenches and to prepare the surface of the substrate (planarization) for the subsequent forming of the inductor (Fig. 1c).

[0010] This technique is, however, very costly in that it requires a long time for forming the trenches (1 μm/min) and moreover with current etching machines it is not possible to carry out the operation simultaneously on a number of wafers, but only on a single wafer at a time.

[0011] An alternative technique that has been proposed recently and that makes it possible to reduce losses due to the substrate is described in "PROCEEDINGS OF THE IEEE", vol. 86, No. 8, August 1998, page 1632, and essentially envisages the creation of a cavity or air gap underneath the inductor by removing the silicon underneath the inductor by means of anisotropic chemical etches made using potassium hydroxide (KOH), tetramethyl ammonium hydroxide (TMAH), etc., and employing a sacrificial polycrystalline-silicon layer.

[0012] This technique is schematically illustrated in Figures 2a-2c, and essentially involves the deposition and definition, using a special mask, of a sacrificial polycrystalline-silicon layer 5 on the top surface of the substrate 1, deposition of a silicon-nitride (Si_3N_4) layer 6 above the sacrificial polycrystalline-silicon layer 5 (Fig. 2a), and then the carrying-out of an anisotropic etch of the substrate 1 through an opening 7 made in the silicon-nitride layer 6 (Fig. 2b). By means of the anisotropic etch, the sacrificial polycrystalline-silicon layer 5 and part of the substrate 1 are thus removed, and a cavity or air-gap 8 is obtained having a roughly triangular cross section, which is separated from the outside environment by a diaphragm 9 consisting of the portion of the silicon-nitride layer 6 overlying the cavity 8, and on which the inductor can subsequently be made.

[0013] This technique presents some drawbacks that do not enable adequate exploitation of all its advantages.

[0014] In the first place, for the formation of the cavity 8 the above technique requires the deposition, and the corresponding definition through a special mask, of a sacrificial polycrystalline-silicon layer 5, with the costs associated thereto.

[0015] In the second place, the said technique does not enable a uniform isolation level to be obtained underneath the inductor, in that isolation is maximum at the centre of the cavity 8 (i.e., at the vertex that is set further down of the triangle) whilst it is minimum at the ends of the cavity 8 (i.e., at the two vertices of the triangle that are set higher up). Consequently, in order to guarantee a minimum level of isolation of the inductor that may be acceptable over the entire extent of the latter, it is typically necessary to provide a cavity, the top area of which is larger than the area of the inductor, with a consequent larger area occupied on the silicon with respect to the one that would be occupied if the known technique illustrated in Figures 1a-1c were instead used.

[0016] The object of the present invention is to provide a process for forming a buried cavity in a semiconductor

material wafer that does not present the limitations of the processes of the known art.

[0017] According to the present invention, a process for forming a buried cavity in a semiconductor material wafer is provided, as defined in Claim 1.

[0018] For a better understanding of the present invention, preferred embodiments thereof are now described, merely to provide non-limiting examples, with reference to the attached drawings, in which:

- Figures 1a-1c show cross sections of a semiconductor material wafer in successive steps of a first known forming process;
- Figures 2a-2c show cross sections of a semiconductor material wafer in successive steps of a second known forming process;
- Figure 3 shows a top view of a semiconductor material wafer in which the cavity has a pre-set orientation with respect to the wafer;
- Figures 4a-4d show cross sections of the wafer of Figure 3 at an enlarged scale in successive forming steps, according to the present invention;
- Figures 5 and 6 show portions of masks used during the forming process according to the present invention; and
- Figures 7a and 7b show cross sections of the wafer of Figure 4d in successive forming steps, according to a different embodiment of the invention.

[0019] Figure 3 shows a wafer in which a cavity or air gap 20 is formed using a holed mask 16 having openings oriented at approximately 45° with respect to the "flat" of the wafer 10, identified by the orientation <110>, as is shown in the detail of Figure 5. The surface of the wafer 10 has, instead, orientation <100>.

[0020] For forming the cavity 20, according to what is illustrated in Figures 4a-4d, directly on the top surface 13 of a P or P+ monocrystalline silicon substrate 11 (i.e., without the interposition of a sacrificial polycrystalline-silicon layer), a first silicon-dioxide layer 12 is initially grown having a thickness of between 200 Å and 600 Å, and a silicon-nitride layer 14 is next deposited thereon having a thickness of between 900 and 1500 Å (Fig. 4a).

[0021] Next, using a resist mask (not shown), dry etching is carried out of the uncovered portions of the silicon-nitride layer 14 and of the silicon-dioxide layer 12, and the resist mask is then removed. In this way, the portions of the silicon-nitride layer 14 and of the silicon-dioxide layer 12 that have remained after the dry etching form the holed mask 16 (Fig. 4b).

[0022] As is illustrated in detail in Figure 5, the holed mask 16 has a lattice structure provided with openings 18 having a substantially square cross section, with sides having a length L1 of, for example, between 1 μm and 3 μm, preferably 2 μm, and an inclination of 45° ±1° with respect to the "flat" of the wafer 10. The openings are set apart at a distance comparable to the length L1, and hence, for example, at a distance of between 1 μm and 3 μm.

[0023] Using the holed mask 16, the substrate 11 is then anisotropically etched under time control in tetramethyl ammonium hydroxide (TMAH), thus forming the cavity 20, which substantially has the shape of an isosceles trapezium turned upside down and a depth of between 50 μm and 100 μm (Fig. 4c).

[0024] In particular, the shape of an upside-down isosceles trapezium of the cavity 20 is obtained thanks to the combination of the following factors: execution of an anisotropic etch; use of a holed mask 16; and orientation at 45° ±1° of the openings 18 with respect to the "flat" of the wafer 10.

[0025] In fact, with the particular combination described above, the individual etches having their origin from the openings 18 of the holed mask 16 are performed on particular crystallographic planes of the silicon which enable the individual etches to "join up" laterally to one another, thus causing removal of the silicon not only in the vertical direction (i.e., in the direction of the depth of the substrate 11), but also in the horizontal direction (width/length), thus leading to the formation of the cavity 20 having the shape shown in Figure 4c.

[0026] If, instead, the openings 18 of the holed mask 16 had sides parallel or orthogonal to the "flat" of the wafer 10, the individual etches having their origin from the opening 18 of the holed mask 16 would be performed on crystallographic planes of the silicon that would not enable the individual etches to "join up" laterally to one another, thus leading to the formation of a set of cavities, equal in number to the openings 18 of the holed mask 16, separate from one another, and each having a cross section shaped like an upside-down triangle, of the same type as that shown in Figure 2c.

[0027] The use of TMAH for carrying out anisotropic etching of the substrate 11 is moreover particularly advantageous in combination with the structure of the holed mask 16 described above for leading to the formation of the cavity 20 having the shape illustrated in Figure 4c, in that also this contributes to lateral joining-up of the individual etches.

[0028] With reference again to Figures 4a-4d, following upon TMAH anisotropic etching, a chemical vapour deposition (CVD) of tetraethyl orthosilicate (TEOS) is carried out for a thickness of 2 μm, which leads to the formation of a coating layer 22, which is thinner and which coats-the side walls and bottom wall of the cavity 20, and of a closing layer 24 which completely closes the openings of the holed mask 16 (Fig. 4d).

[0029] The closing layer 24 defines, on top of the cavity 20, a diaphragm 26, above which, in a way in itself known and not illustrated, the suspended structure can then made, such as an inductor, a resistor, etc.

[0030] The advantages of the process according to the present invention are described in what follows.

[0031] In the first place, forming cavities according to the present invention does not entail the deposition, and

the corresponding definition through a dedicated mask, of a special polycrystalline-silicon layer; the fabrication process is consequently simpler and more economical, thanks to the reduction in the number of the steps required, and in particular to the elimination of the mask necessary for the definition of the sacrificial polycrystalline-silicon layer.

[0032] In the second place, the process described enables the fabrication of a cavity 20 the shape of which makes it possible to achieve a uniform isolation level beneath the electronic component (inductor, resistor, etc.) made on the diaphragm 26 overlying the cavity 20, thus reducing occupation of the area on silicon with respect to that which there would be if the prior art techniques shown in Figures 2a-2c were used.

[0033] In addition, the present process can be employed for the formation of cavities having, in plan view, any shape whatsoever, and even elongated cavities defining true buried channels.

[0034] Finally, it is clear that numerous modifications and variations can be made to the process described and illustrated herein, without thereby departing from the sphere of protection of the present invention, as defined in the attached claims.

[0035] For example, the holed mask used in the process could also present a different pattern of the openings. For instance, it is possible to use the pattern shown in Figure 6, in which the holed mask 16' has openings 18' having a substantially rectangular shape, with the smaller side having a length L1 of, for example, between 1 μm and 3 μm, preferably 2 μm, and the larger side having a length L2 of, for example, between 1 μm and 10 μm, preferably 5-7 μm, and an inclination of 45° ±1° with respect to the "flat" of the wafer 10. The distance between the openings 18' is preferably comparable with that of the smaller side L1, and is hence, for example, between 1 μm and 3 μm.

[0036] In addition, the openings 18' are arranged in parallel rows, and the openings 18' belonging to adjacent rows are staggered with respect to one another.

[0037] Furthermore, the openings 18' could present a shape slightly different from that illustrated in Figure 6. In particular, they could present any shape elongated along a prevalent direction having the inclination referred to above with respect to the "flat" of the wafer 10, for example the shape of a flattened ellipse, a generally quadrangular elongated shape, etc.

[0038] Finally, the same process can be used to make buried channels connected with the outside world at communication openings, for example elongated channels having two opposite ends and being connected via communication openings set at the ends of the channels themselves. In this case, the openings 18, 18' of the holed mask 16, 16' are arranged so as to obtain the desired shape for the cavity 20 or for a plurality of cavities 20. In addition, instead of depositing TEOS after the formation of the cavity 20, polycrystalline silicon is deposited, which comes to form the coating layer 22 and the closing layer 24. Next, as shown in Figure 4a, an epitaxial layer 30 is grown so as to strengthen the diaphragm 26. Finally, using known etching techniques, the openings 31 are made at the two ends of the cavity or of each cavity 20 (Figure 7b), so as to form areas of access to the cavity or cavities 20. This solution is particularly suited for the fabrication of microreactors for the DNA chain reaction.

Claims

1. A process for forming a buried cavity (20) in a semiconductor material body (11), comprising the steps of:

   - forming a mask (16) on top of said semiconductor material body (11); and
   - anisotropically etching said semiconductor material body (11) using said mask (16);

   characterized in that said mask (16) has a plurality of openings (18; 18'), each having a side or a prevalent direction with an inclination of between 44° and 46° with respect to a flat (100) of said semiconductor material body (11).

2. The process according to Claim 1, **characterized in that** said openings (18) have a side or a prevalent direction with an inclination of 45° with respect to said flat (100) of said semiconductor material body (11).

3. The process according to Claim 1 or Claim 2, **characterized in that** said openings (18; 18') have a quadrangular shape.

4. The process according to Claim 3, **characterized in that** said openings (18) have a substantially square shape.

5. The process according to Claim 3, **characterized in that** said openings (18') have a substantially rectangular shape.

6. The process according to Claim 5, **characterized in that** said openings (18') are arranged in parallel rows.

7. The process according to Claim 6, **characterized in that** said openings (18') belonging to adjacent rows are staggered with respect to one another.

8. The process according to any of the foregoing claims, **characterized in that** said mask (16) has a lattice structure.

9. The process according to any of the foregoing

claims, **characterized in that** said mask (16) is made directly above a surface (13) of said semiconductor material body (11).

10. The process according to any of the foregoing claims, **characterized in that** said -anisotropic etching step is carried out using TMAH.

11. The process according to any of the foregoing claims, **characterized in that** said anisotropic etching step is time-controlled.

12. The process according to any of the foregoing claims, characterized by the further step of:

- forming, above said mask (16), a coating layer (22) closing said openings (18; 18').

13. The process according to Claim 12, **characterized in that** said step of forming a coating layer (22) comprises carrying out TEOS chemical vapour deposition.

14. The process according to Claim 12, **characterized in that** said step of forming a coating layer (22) comprises the deposition of a polycrystalline-silicon layer.

15. The process according to Claim 13, characterized by the further steps of growing an epitaxial layer (30) on said coating layer and of forming communication openings (31) extending in said epitaxial layer (31) and in said coating layer as far as said cavity (20).

16. The process according to any of the foregoing claims, **characterized in that** said mask (16) is a hard mask comprising oxide portions (12) in contact with said semiconductor material body (11) and silicon-nitride portions (14) above said oxide portions (12).

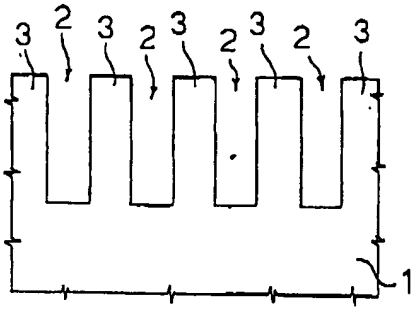

Fig. 1a

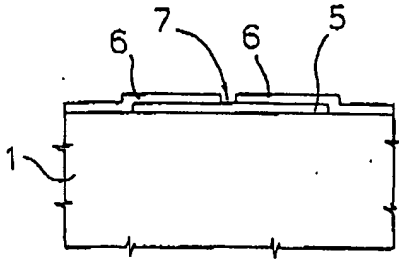

Fig. 2a

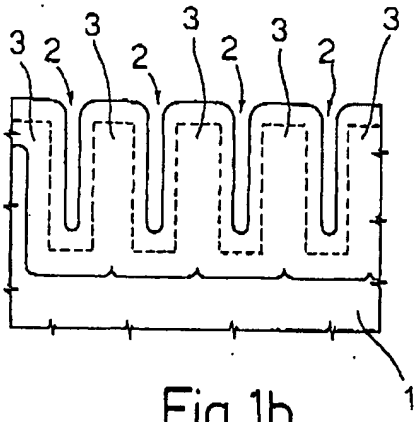

Fig. 1b

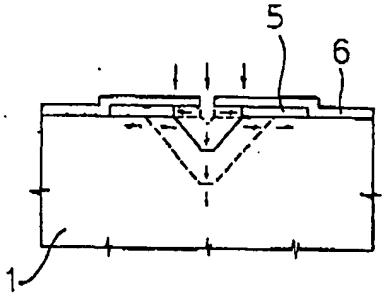

Fig. 2b

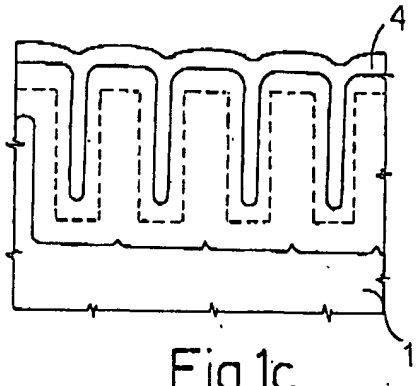

Fig. 1c

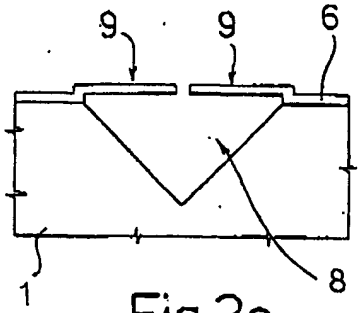

Fig. 2c

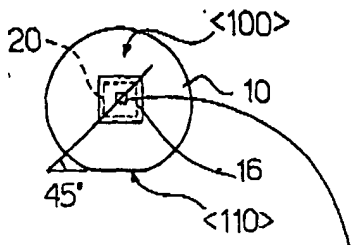

Fig.3

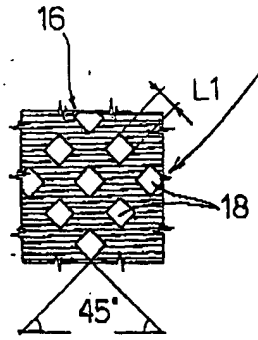

Fig.5

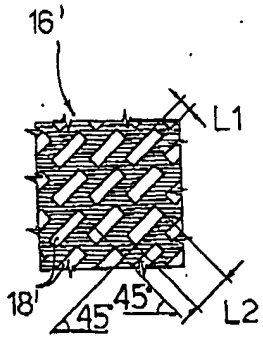

Fig.6

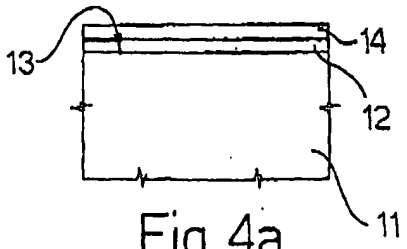

Fig. 4a

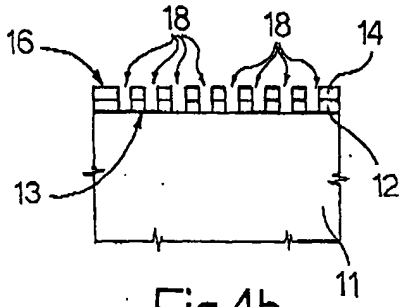

Fig.4b

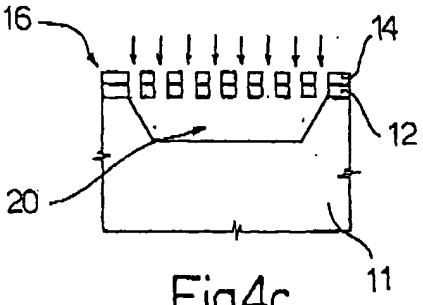

Fig.4c

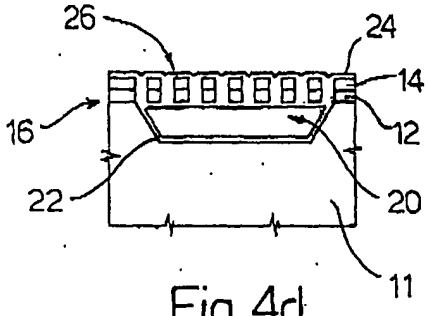

Fig.4d

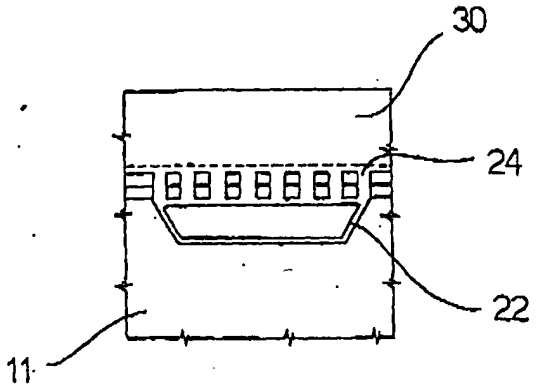

Fig. 7a

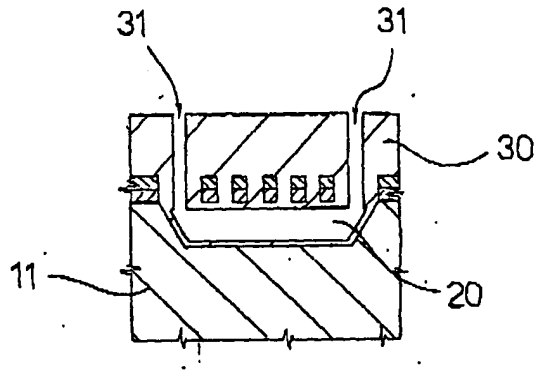

Fig. 7b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0148

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X A	DE 196 21 349 A (ZENTRUM MIKROELEKTRONIK DRESDE) 4 December 1997 (1997-12-04) * column 1, line 39 - line 64 * * column 5 - column 8; figures 1,2 * ---	1-3,9,11 5,10,16	H01L21/308
Y	EP 0 658 927 A (ANT NACHRICHTENTECH) 21 June 1995 (1995-06-21) * the whole document * ---	1-5,9,11	
Y	"METHOD OF MAKING SEPARATE REGIONS OF VARIOUS AVERAGE DEPTHS WITH ONE ANISOTROPIC ETCH" RESEARCH DISCLOSURE,GB,INDUSTRIAL OPPORTUNITIES LTD. HAVANT, no. 316, 1 August 1990 (1990-08-01), pages 688-689, XP000141023 ISSN: 0374-4353	1-5,9,11	
A	* the whole document * ---	6-8	
A	DATABASE WPI Section Ch, Week 199812 Derwent Publications Ltd., London, GB; Class L03, AN 1998-128965 XP002144373 & SE 9 601 777 A (IMC INDUSTRIELLT MIKROELEKTRONIKCENTRUM), 10 November 1997 (1997-11-10) * abstract * -& SE 513 072 C (ACREO AB) 3 July 2000 (2000-07-03) * page 3 - page 5; figures 1-6 * --- -/--	1,3-5, 10,12, 13,16	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L B81C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	4 August 2000	Szarowski, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

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EUROPEAN SEARCH REPORT

Application Number
EP 00 83 0148

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	ZOU Q B ET AL: "SINGLE-CHIP FABRICATION OF INTEGRATED FLUID SYSTEMS (IFS)" IEEE WORKSHOP ON MICRO ELECTRO MECHANICAL SYSTEMS,US,NEW YORK, NY: IEEE, 25 January 1998 (1998-01-25), pages 448-453, XP000829203 ISBN: 0-7803-4413-8 * page 448 - page 450 *	1,3,5,6, 8,11-13	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

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Place of search	Date of completion of the search	Examiner
THE HAGUE	4 August 2000	Szarowski, A

CATEGORY OF CITED DOCUMENTS

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